IMAGE PROCESSING APPARATUS

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is based on application No. 11-328130
filed in Japan, the contents of which are hereby incorporated
by reference.

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The present invention relates to an image processing
apparatus for processing image data, and more particularly, to
an image processing apparatus using a rewritable device.

DESCRIPTION OF THE RELATED ART

A real-time image processing apparatus optimally
processes image data read by a one-dimensional image sensor of
a reader in real time, and sends the processed image data to
an outputter. Here, a plurality of line memories (for example,
FIFO memories) are used in an image processing circuit mainly
using a spatial filter. The size, the number and the
configuration of the line memories are univocally decided by
a predetermined image processing condition, for example, the
image quality, the output image size or the reading rate
depending on the reading resolution of the image sensor, or the
processing speed required in accordance with the printer system

speed. The circuit configuration associated with the line
memories and the image processing algorithm are similarly
univocally decided. Therefore, when the user changes the image
processing condition such as the image quality, the output image

5   size or the processing speed, since the configuration of the
line memories for image processing and the image processing
algorithm are always the same, there are cases where optimal
image processing is not performed to degrade the image quality.
Moreover, even when it is intended to output a high-quality

10   image, since the configuration of the line memories for image
processing and the image processing algorithm are always the
same, the image quality cannot be increased to the desired one.

OBJECTS AND SUMMARY

15   An object of the present invention is to provide an image
processing apparatus in which the configurations of the line
memories and the circuit associated therewith and the image
processing algorithm can be changed in accordance with the image
processing condition such as the required image quality,

20   processing speed or output image size.

An image processing apparatus according to a first aspect
of the invention is provided with: a pixel matrix formation
section consist of a device that has a rewritable circuit
configuration, and having a plurality of line memories that

25   output pixel data in parallel; a filtering circuit consist of

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a device that has a rewritable circuit configuration, and performing filtering of pixel data by use of a pixel matrix based on the pixel data received in parallel from the line memories; a memory for storing setting information for rewriting the configurations of the devices; and a controller for rewriting the configuration of the line memories and the configuration of the filtering circuit by use of the setting information stored in the memory based on an image processing condition.

An image processing apparatus according to a second aspect of the invention is provided with: a processing circuit having a plurality of line memories and performing filtering of pixel data by use of a pixel matrix based on pixel data from the line memories; a memory for storing setting information for rewriting the configuration of the processing circuit; and a controller for rewriting the configuration of the line memories of the processing circuit and the configuration of filtering by use of the setting information stored in the memory based on an image processing condition.

An image processing apparatus according to a third aspect of the invention is provided with: a first circuit consist of a device that has a rewritable configuration, and having a plurality of line memories; a second circuit for processing image data output from the line memories; a memory for storing setting information for rewriting the configuration of the first circuit; and a controller for rewriting the configuration

of the line memories of the first circuit by use of the setting information stored in the memory based on an image processing condition.

　　　These and other objects, advantages and features of the invention will become apparent from the following description thereof taken in conjunction with the accompanying drawings which illustrate specific embodiments of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram showing the general configuration of a color image processing circuit;

FIG. 2 is a block diagram showing the configuration of a part of an area determination section;

FIG. 3 is a block diagram showing the configuration of another part of the area determination section;

FIG. 4 shows the image reading ranges of a processing speed priority mode and an image quality priority mode;

FIG. 5 shows a relationship between the sizes of an isolated point detection filter and isolated points in the processing speed priority mode;

FIG. 6 shows a relationship between the sizes of the isolated point detection filter and the isolated points in the image quality priority mode;

FIG. 7 shows the dot area determination ranges of the modes;

FIG. 8 shows the configuration of a matrix formation section and an isolated point detection section in the processing speed priority mode;

FIG. 9 shows the configuration of the matrix formation section and the isolated point detection section in the image quality priority mode; and

FIG. 10 shows an example of calculation of the dot determination threshold values of the modes.

In the following description, like parts are designated by like reference numbers throughout the several drawings.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Hereinafter, an embodiment of the present invention will be described with reference to the accompanying drawings. In the figures, like reference numbers designate like parts.

FIG. 1 shows the general circuit configuration of a color image processing apparatus. The red, green and blue output signals of a color CCD sensor 10 comprising line sensors of three colors are converted into digital signals by an A/D conversion section 12. The obtained red (R), green (G) and blue (B) digital image data are corrected by a shading correction section 14 and supplied to a scaling and movement section 16, where scaling and movement of the image data are performed. The output image data from the scaling and movement section 16 are converted into print colors of cyan (C), magenta (M), yellow (Y) and black (Bk)

by a color correction section 18, and determination of areas is performed by an area determination section 20. An MTF correction section 22 corrects the image data output from the color correction section 18 in accordance with the result of

5 the area determination by the area determination section 20, and outputs the corrected image data to a printer. The user can set, with an operation panel 28, the image processing condition such as the output image size (output sheet size), a processing speed priority mode or an image quality priority

10 mode.

In the color image processing circuit, the area determination section 20 comprises a device having a rewritable circuit configuration such as a field programmable gate array (FPGA). The FPGA is an integrated circuit in which the logic

15 circuit is reconstructed based on predetermined setting information. The image processing function is reconstructed by this integrated circuit. The setting information used in the reconstruction of the image processing function is stored in a ROM 26. A CPU 24 reconstructs the image processing function

20 of the area determination section 20 by using the setting information stored in the ROM 26 or a processing circuit program in accordance with the set image processing condition such as the mode or the output size. Consequently, the circuit configuration of the area determination section 20 is rewritten,

25 so that the image processing algorithm is changed.

Specifically, in the area determination section 20, a filtering circuit and line memories (for example, FIFO memories) for forming a pixel matrix are formed by using the FPGA, and the configuration of the line memories (the lateral size and the number of lines) and the configuration of the filtering circuit are changed in accordance with the set image processing condition such as the output size or the mode.

FIGs. 2 and 3 show the configuration of the area determination section 20. For simplicity, only determination of a dot area will be described. First, by an MIN circuit 200, lightness (V) data which is the minimum value of red, green and blue input image data RIN, GIN and BIN is obtained for each pixel from the data RIN, GIN and BIN. Then, at a matrix formation section 202, the lightness data successively input in units of pixels are held in a plurality of cascaded line memories, and the lightness data are paralelly read from the line memories, thereby extracting a pixel matrix. An isolated point detection section 204 detects whether the pixel of interest of the pixel matrix of the lightness (V) data extracted at the matrix formation section is a black or a white isolated point or not based on the pixel matrix, and produces a black isolated point signal KAMI or a white isolated point signal WAMI. The detection as to whether the pixel is an isolated point or not is performed for each pixel. For the pixels detected to be isolated points, the black isolated point signal KAMI or the

white isolated point signal WAMI becomes high. For the pixels

not detected to be isolated points, the black isolated point

signal KAMI or the white isolated point signal WAMI becomes low.

The processing algorithms of the matrix formation section 202

5   and the isolated point detection section 204 are reconstructed

by the CPU 24 through a CPU bus based on the setting information

stored in the ROM 26. Then, the signals KAMI and the signals

WAMI obtained for the pixels are developed into 9×41 matrices

206 and 208, respectively, and the number of black and white

10   isolated points, that is, the number of pixels determined to

be isolated points is counted by counter sections 210 and 212

to produce the number of black isolated points KOUT and the

number of white isolated points WOUT.

Then, the obtained numbers of isolated points KOUT and WOUT

15   are compared with black and white dot determination threshold

values (KTh, WTh) by comparators 214 and 216, respectively. The

numbers of isolated points KOUT and WOUT are added by an adder

218, and the sum is compared with a dot determination threshold

value (TTh) by a comparator 220. When any of the comparison

20   results is effective (low level), an OR gate 222 determines that

the pixels constitute a dot area.

Next, the processing speed priority mode and the image

quality priority mode set with the operation panel 28 will be

described. When the processing speed priority mode is selected,

25   speed-oriented image processing is performed. When the image

quality priority mode is selected, quality-oriented image processing is performed.

FIG. 4 shows the image reading areas of these modes. In the processing speed priority mode, the original is set in landscape orientation for readout. When the resolution is 600 dpi and the size is A4 in landscape orientation, the data amount is 7,500 pixels per line in the main scanning direction. The scan time is shorter than that of A4 in portrait orientation. In the image quality priority mode, the original is set in portrait orientation for readout. When the resolution is 600 dpi and the size is A4 in portrait orientation, the data amount is 5,000 pixels per line in the main scanning direction. The scan time is longer than that of A4 in landscape orientation. Therefore, the contents of the line memories (FIFO memories) are changed in accordance with the data amount per line. Specifically, in the processing speed priority mode, $8k \times 8$-bit FIFO memories are constructed, and in the image quality priority mode, $5k \times 8$-bit FIFO memories are constructed.

The number of line memories (FIFO memories) is also changed in accordance with the mode. In the image quality priority mode, six FIFO memories are constructed for forming a 7×7-pixel isolated point detection filter. In the processing speed priority mode, four FIFO memories are constructed for forming a 5×5-pixel isolated point detection filter. In the image quality priority mode, the isolated point detection filter is

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larger than that in the processing speed priority mode, and the time required for its computation is longer than that in the processing speed priority mode. In the image quality mode, since the isolated point detection filter is large, the accuracy

5   of the isolation point detection is higher than that in the processing speed priority mode, so that the quality of the processed image is improved.

As described above, the configuration of the line memories in the matrix formation section 202, that is, the capacity of

10   each line memory and the number of line memories are rewritten according to the mode. When the mode is changed with the operation panel 28, the CPU 24 reconstructs the configuration of the line memories in the matrix formation section 202 by use of the setting information in the ROM 26.

15   FIGs. 5 and 6 show the relationships between the sizes of the isolated point detection filter and the isolated point (hatched part) in the processing speed priority mode and in the image quality priority mode. In the processing speed priority mode (FIG. 5), since a 5×5-pixel filter is used for a pixel

20   size of 600 dpi, an isolated point forming a dot of 85 L (L is a unit representative of the number of lines per inch, line/inch) is larger than the filter (FIG. 5(b)), so that the isolated point cannot be recognized. Only when forming a dot of not less than 100 L (FIG. 5(a)), an isolated point can be

25   recognized and the dot area can be determined. On the contrary,

in the image quality priority mode (FIG. 6), since a 7×7-pixel
filter is used for a pixel size of 600 dpi, an isolated point
forming a dot of 85 L is not larger than the filter, so that
the isolated point can be recognized. Likewise, an isolated

5   point forming a dot of 65 L can be recognized. Thus, all the
dot areas can be determined. FIG. 7 shows the dot area
determination ranges of the modes. In the processing speed
priority mode, the accuracy of the dot area determination is
narrow and the dot area cannot be determined at 65L and 85L,

10   so that image quality degradation (moiré pattern, etc.) occurs.
In the image quality priority mode, all the dot areas can be
determined, so that the image quality is excellent.

The circuit configuration of the area determination
section 20 in accordance with the set mode and the output image

15   size (sheet size) is reconstructed by the CPU 24 based on the
setting information stored in the ROM 26. Specifically, the
configuration of the line memories of the matrix formation
section 20 and the circuit configuration of the isolated point
detection section are reconstructed in accordance with the

20   output image size and the mode. By thus rewriting the circuit
configuration of the matrix formation section 202 and the
circuit configuration of the isolated point detection section
204, the image processing accuracy can be changed, so that the
image quality can be improved.

25   FIG. 8 shows the circuit contents of a matrix formation

section 202A and an isolated point detection section 204A

constructed in the processing speed priority mode. Since the

image data is 8-bit data of A4 size in landscape orientation

and with a resolution of 600 dpi, FIFO memories of one line

5 require a capacity of $8k \times k$ bits. Moreover, since a 5×5-pixel

filter is used, four FIFO memories 2020A are cascaded in the

matrix formation section 202A. As pixel data V1 of the first

line, the input pixel data is output as it is. Consequently,

pixel data V1, V2, V3, V4 and V5 of five lines are output in

10 parallel from the matrix formation section 202A.

The isolated point detection section 204A successively

receives the pixel data V1, V2, V3, V4 and V5 in parallel from

the matrix formation section 202A, and extracts a 5×5 pixel

matrix 2040A. Here, Vi, j ($1 \leqq i$, $j \leqq 5$) represents data of a

15 pixel (i, j). Then, for the 5×5 matrix, the condition of

peripheral pixels of the pixel of interest situated at the

center is examined by filtering sections 2042A and 2044A, and

pixels of interest satisfying the conditions of determination

of white and black isolated points shown in the figure, that

20 is, white and black isolated points are detected. For the

pixels detected to be isolated points, the black isolated point

signal KAMI or the white isolated point signal WAMI becomes high.

For the pixels not detected to be isolated points, the black

isolated point signal KAMI or the white isolated point signal

25 WAMI becomes low.

FIG. 9 shows the contents of a matrix formation section 202B and an isolated point detection section 204B constructed in the image quality priority mode. Since the image data of interest in this mode is 8-bit data of A4 in portrait orientation and with a resolution of 600 dpi, FIFO memories of one line require a capacity of 5k×8 bits. Moreover, six FIFO memories 2020B are cascaded for forming a 7×7-pixel isolated point detection filter. As pixel data V1 of the first line, the input pixel data is output as it is. Consequently, pixel data V1, V2, V3, V4, V5, V6 and V7 of seven lines are output in parallel from the matrix formation section 202B.

The isolated point detection section 204B successively receives the pixel data V1, V2, V3, V4, V5, V6 and V7 in parallel from the matrix formation section 202B, and extracts a 7×7 pixel matrix 2040B. Here, $V_{i,j}$ ($1 \leqq i$, $j \leqq 7$) represents data of a pixel (i, j). Then, after the 7×7 pixel matrix 2040B is smoothed by use of a 5×3-pixel smoothing filter 2042B, a 5×5 pixel matrix 2044B is extracted from the smoothed data $S_{i,j}$. In the case of a white isolated point, the condition of peripheral pixels of the pixel of interest is examined by use of the pixel matrices 2040B and 2044B, and the white isolated point that satisfies the condition of the white isolated point (WAMI="H") shown in the figure is obtained by a filtering section 2046B. In the case of a black isolated point, the condition of peripheral pixels of the pixel of interest is

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examined by a filtering section 2048B by use of the pixel

matrices 2040B and 2044B based on the condition shown in the

figure, and the black isolated point that satisfies the

condition of the black isolated point (KAMI="H") shown in the

5   figure is obtained. For the pixels detected to be isolated

points, the black isolated point signal KAMI or the white

isolated point signal WAMI becomes high. For the pixels not

detected to be isolated points, the black isolated point signal

KAMI or the white isolated point signal WAMI becomes low.

10   Moreover, the area determination section 20 is rewritten

in accordance with the output image size (output sheet size)

set with the operation panel 28. For example, when A4 in

landscape orientation is set as the output image size, the

circuit configuration shown in FIG. 8 is constructed, and when

15   A4 in portrait orientation is set as the output image size, the

circuit configuration shown in FIG. 9 is constructed.

Description of the contents of FIGs. 8 and 9 is omitted as it

has already been given.

FIG. 10 shows an example of calculation of the dot

20   determination threshold values of the modes. In the image

quality priority mode, in theory, there are 22 isolated points

detected by the isolated point detection section by use of the

7×7 pixel matrix in a 9×41 pixel matrix. Therefore, the

threshold value for the image quality priority mode is 22.

25   With the above-described embodiment, the circuit

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configuration associated with filtering in the image processing circuit can be reconstructed in accordance with the image processing condition required by the user. Consequently, the image processing algorithm can be changed in accordance with

5　various image processing conditions, so that the quality of the output image can be improved.

Although the present invention has been fully described by way of examples with reference to the accompanying drawings, it is to be noted that various changes and modification will

10　be apparent to those skilled in the art. Therefore, unless otherwise such changes and modifications depart from the scope of the present invention, they should be construed as being included therein.